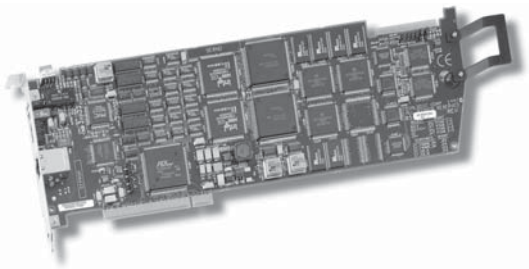
Datasheet

Intel® Dialogic® D/240PCI-T1, D/240SC-T1, D/300PCI-E1, and D/300SC-E1 Voice Boards

24- and 30-Port Voice Processing with Digital Network Interface

Retired products — This datasheet is for informational purposes only; the products detailed in this datasheet are no longer available. Consider migrating to the Intel® Dialogic® D/240JCT-T1 or D/300JCT-E1 combined media boards.

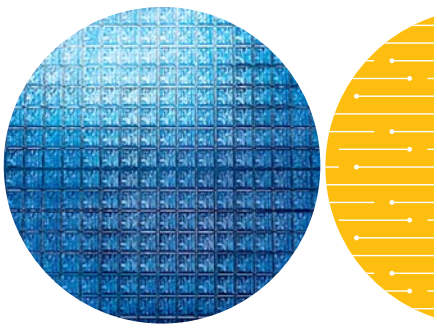
The Intel® Dialogic® D/240PCI-T1, D/240SC-T1, D/300PCI-E1, and D/300SC-E1 voice boards are ideal for developers seeking to provide cost-effective, highly scalable, high-density computer telephony (CT) solutions for voice processing applications requiring ISDN Primary Rate service termination plus 24 (T-1) or 30 (E-1) voice ports in a single PC slot. A number of different boards are available. A unique multiprocessor architecture comprising of digital signal processors (DSP) and general-purpose microprocessors handles all telephony signaling and performs all DTMF (touch-tone) and audio/voice signal processing tasks.



Intel in Communications

Features and Benefits

- High channel-per-slot density: one T-1 ISDN PRI span with 24 channels of voice processing or one E-1 ISDN PRI span with 30 channels of voice processing
- Offered in both PCI and ISA form factors
- PCI boards have a CT Bus that operates in SCbus mode; ISA boards have an SCbus with PEB connector and can also interoperate with PCI boards using CT/SCbus adapter
- Spring Ware downloadable signal and call processing firmware provides easy feature enhancement and field-proven performance based on over ten million installed ports
- Unified call control access through Global Call interface provides worldwide application portability and shortens development time by using the same API for almost any network protocol
- Intel NetMerge® Converged Communications Software support facilitates multiapplication development
- Supports SNMP agent software for remote CT board management
- Enables system integrators and developers to lower costs by incorporating more ports per chassis, using less expensive desktop-style machines, and easing configuration/installation effort
- Software Development Kits (SDKs) for Windows NT*, Windows 2000*, and Linux* yield faster time to market



Model	Channels	Interface Factor	Form Bus	Resource Support	OS Type	Connector
D/240PCI-T1	24	1 T-1	ISA	PCI (operating in SCbus mode) CT Bus	Windows NT Windows 2000 Linux	RJ-48C
D/240SC-T1	24	1 T-1	ISA	SCbus (with PEB connectors)	Windows NT Windows 2000 Linux	RJ-48C
D/300PCI-E1	30	1 E-1	ISA	PCI (operating in SCbus mode) CT Bus	Windows NT Windows 2000 Linux	BNC (75 Ohm) RJ-48C (120 Ohm)
D/300SC-E1	30	1 E-1	ISA	SCbus (with PEB connectors)	Windows NT Windows 2000 Linux	BNC (75 Ohm) RJ-48C (120 Ohm)

These boards are available in both PCI and ISA form factors. PCI models incorporate a CT Bus connector that operates in SCbus mode.

Onboard DSPs provide variable voice encoding at bit rates of 24 Kb/s and 32 Kb/s for adaptive differential pulse code modulation (ADPCM) and bit rates of 48 Kb/s and 64 Kb/s μ-law or A-law for pulse code modulation (G.711 PCM). Sampling rates and coding methods are selectable on a channel-by-channel basis. Applications may dynamically switch sampling rate and coding method to optimize data storage or voice quality as the need arises. Spring Ware firmware also provides reliable DTMF detection, DTMF cut-through, and talk off/play off suppression over a wide variety of telephone line conditions.

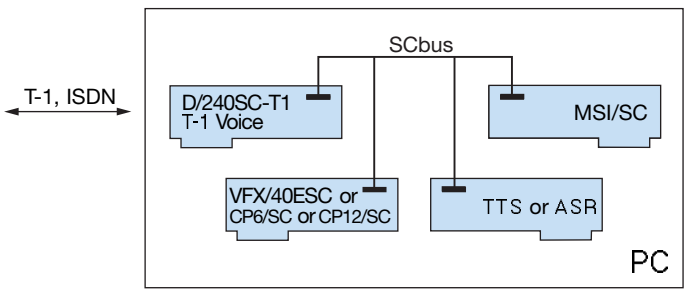
Intel® voice products offer a rich set of advanced features, including DSP technology and signal processing algorithms, for building the core of any computer telephony (CT) system. You can integrate voice products easily into exactly the type of system you require.

In real time, on all channels, these single span PCI and ISA voice boards can

- Connect to 24 T-1 or 30 E-1 telephone channels
- Automatically answer calls
- Detect touch-tones
- Play voice messages to a caller
- Digitize, compress, and record voice signals
- Place outbound calls and automatically report the results

Configurations

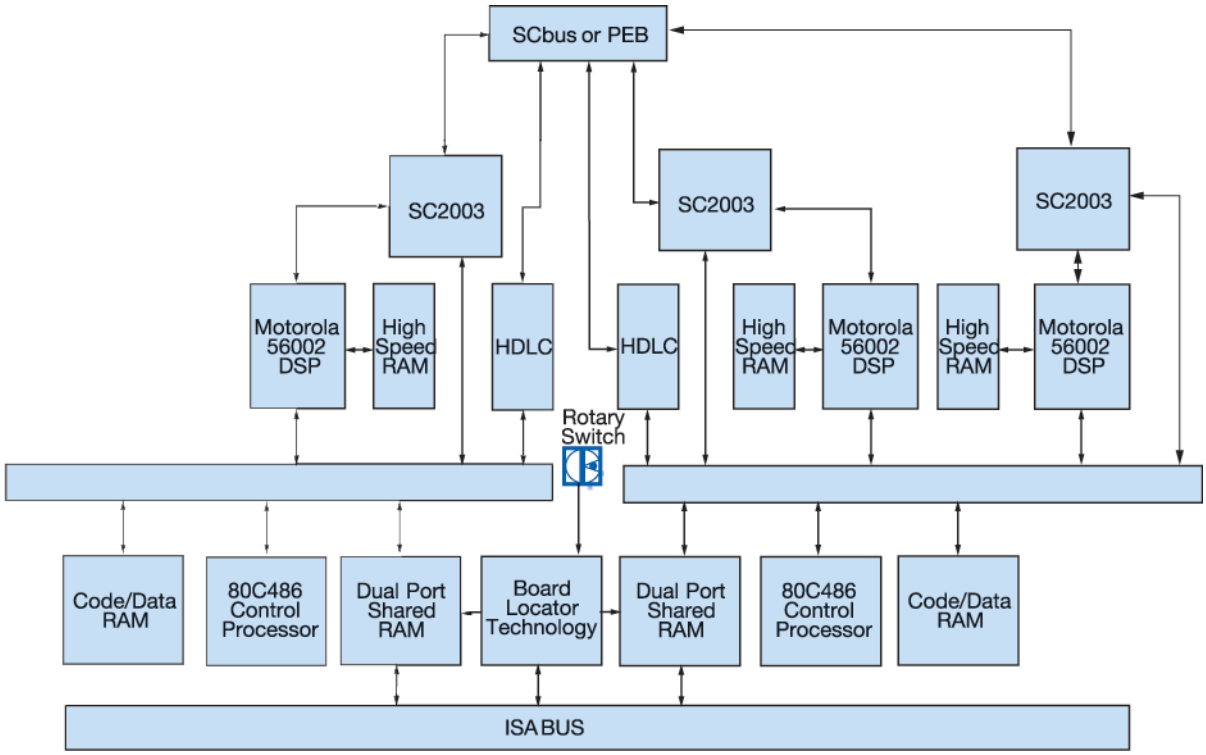
Use single span PCI and ISA boards to develop sophisticated, multifunction computer telephony (CT) systems incorporating capabilities such as voice processing and text-to-speech (TTS). These single span PCI and ISA boards share a common hardware and firmware architecture with other SCbus boards for maximum flexibility and scalability. Add features or grow



Terminate Configuration

Applications

- Messaging
- Contact center and e-Business
- PC-PBX
- Switching and call completion
- Prepaid/debit card
- Gateway switch



Drop-and-Insert Configuration

the system while protecting investment in hardware and application code. Applications can be ported to lower or higher line-density platforms with only minimum modifications.

- Single span PCI boards install in any PCI-based personal computer or server. Each board occupies a single expansion slot and up to 16 boards can be configured in a system
- Single span ISA boards install in IBM PC AT* and compatible computers (PC platforms based on Intel386™, Intel486™, and Pentium® processors). Each board occupies a single expansion slot and up to 16 boards can be configured in a system with each board sharing the same interrupt level.

In either case, PCI or ISA, the number of boards and channels supported depends on the operating system used. The maximum number of lines that can be supported depends on the application type, the amount of disk I/O required, the host computer's CPU(s), and the power supply.

Single span PCI and ISA boards can operate in either terminate or drop-and-insert configurations. In a terminate configuration, the board handles the call processing of the digital audio and telephony signaling. If additional resources such as facsimile, TTS, or ASR are required, the resources can be switched to the call via the SCbus. When single span PCI and ISA boards are installed as a terminating device, no external channel bank is required and the system operates as a standalone call-processing node.

In a drop-and-insert configuration, a single span PCI or ISA board and a digital telephony interface (DTI) board are connected via the SCbus and continuously pass all T-1 or E-1 time slots through to each other. This configuration can join two separate T-1 or E-1 lines, or it can be placed in-line between a T-1 or E-1 line and a switch (a private branch exchange [PBX], for example). Calls on individual channels can either terminate at a call processing resource on the single span PCI or ISA board, or "flow through" transparently from the single span board to the DTI board.

Software Support

Single span PCI and ISA boards are supported by System Software and Software Development Kits for Windows NT*, Windows* 2000, and Linux*. These packages contain a set of tools for developing sophisticated, multimedia communications applications.

Single span PCI and ISA boards can use Global Call software as well as support Intel NetMerge® Converged Communications Software which facilitates multi-application development. These boards also support an SNMP-compatible software for remote CT board management. This agent software simplifies the management of CT devices and lowers the total cost of operation. Centralized management capabilities provide a single point of configuration and inventory for all network devices. Fault management for high availability systems includes diagnostics, detection, and recovery capabilities.

ISDN-PRI Support

PRI firmware from Intel is approved for use with many popular protocols in major market segments, based on both T-1 (1.544 Mb/s) and E-1 (2.048 Mb/s) physical interfaces.

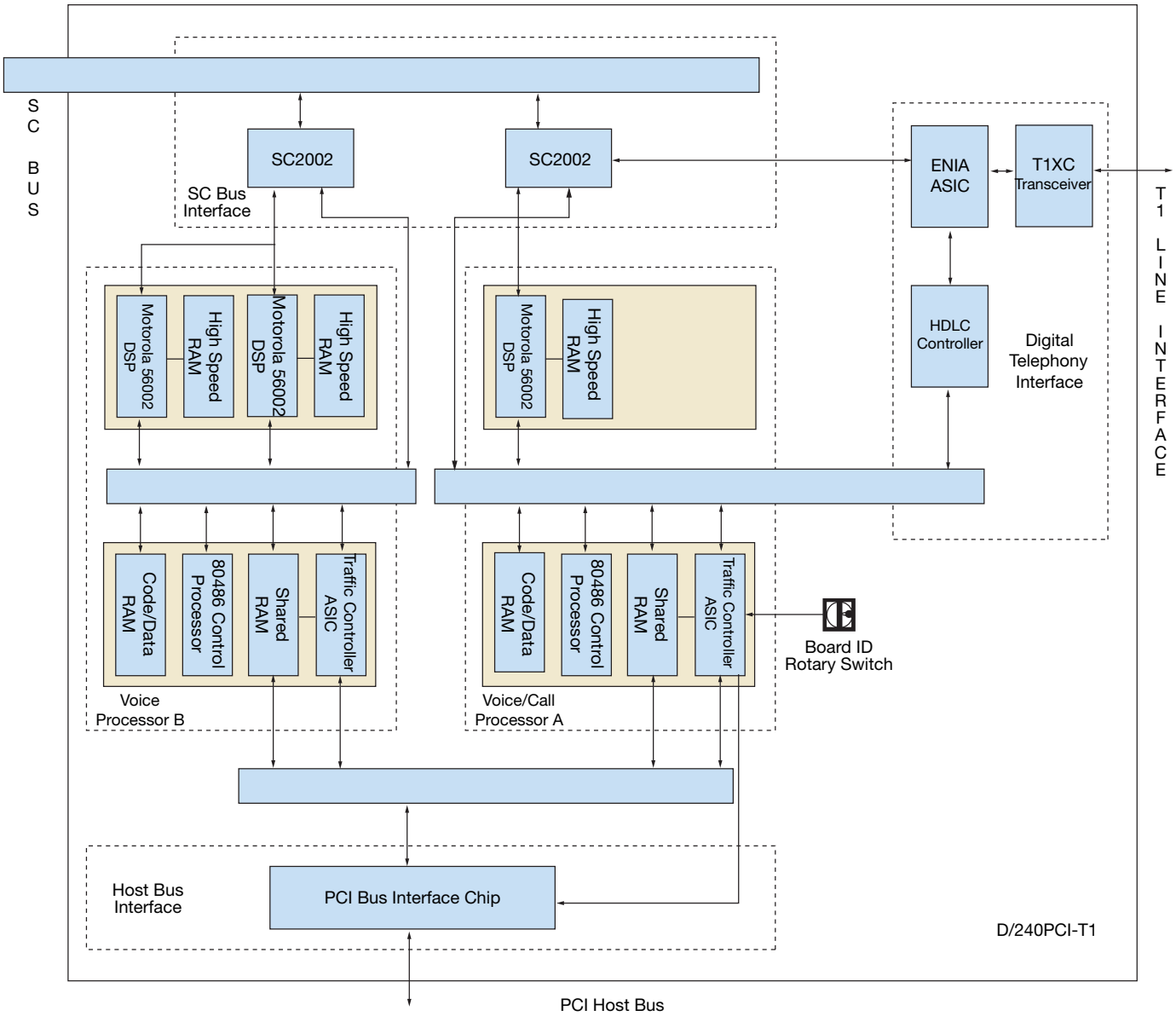
Features and benefits of ISDN PRI include

- ISDN Primary Rate connectivity to CT systems
- Dialed Number Identification Service (DNIS) lets the application route incoming calls by automatically identifying the number the caller dialed
- Automatic Number Identification (ANI) lets the application identify the calling party
- ANI-on-Demand feature saves money by selectively requesting ANI information only when needed
- ISDN offers inherent benefits to call center applications with its fast call setup and fast retrieval of DNIS and ANI information on inbound calls
- Call-By-Call Service Selection lets an application select the most efficient bearer channel service on a call-by-call basis
- Subaddressing allows direct connection to individual extensions or devices sharing the same phone number or as a proprietary messaging mechanism
- Powerful and universal software application programming interface (API) simplifies access for developers who are unfamiliar with ISDN, yet permits sophisticated control of features
- Multinational approvals with many popular protocols
- User-to-User Information lets an application send proprietary messages to remote systems during call establishment
- Facility, Notify, and optional Information Elements (IEs) let applications work with network-specific supplementary services

Global Call

Global Call software provides a common signaling interface for network-enabled applications, regardless of the signaling protocol needed to connect to the local telephone network. Global Call is the recommended API for unified call control for Spring Ware and DM3 architectures. The signaling interface provided by Global Call facilitates the exchange of call control messages between the telephone network and virtually any network-enabled application. Global Call lets developers create an application that can work with signaling systems worldwide, regardless of the network to which they are connected.

Global Call is ideal for high-density, network-enabled solutions for voice, data, and video, where the supported hardware and signaling technology can vary widely. Rather than requiring the application to handle the low-level details, Global Call software offers a consistent, high-level interface to the user, handling each country's unique protocol requirements in a way that is transparent to the application.



D/240PCI-T1 Block Diagram

Functional Descriptions

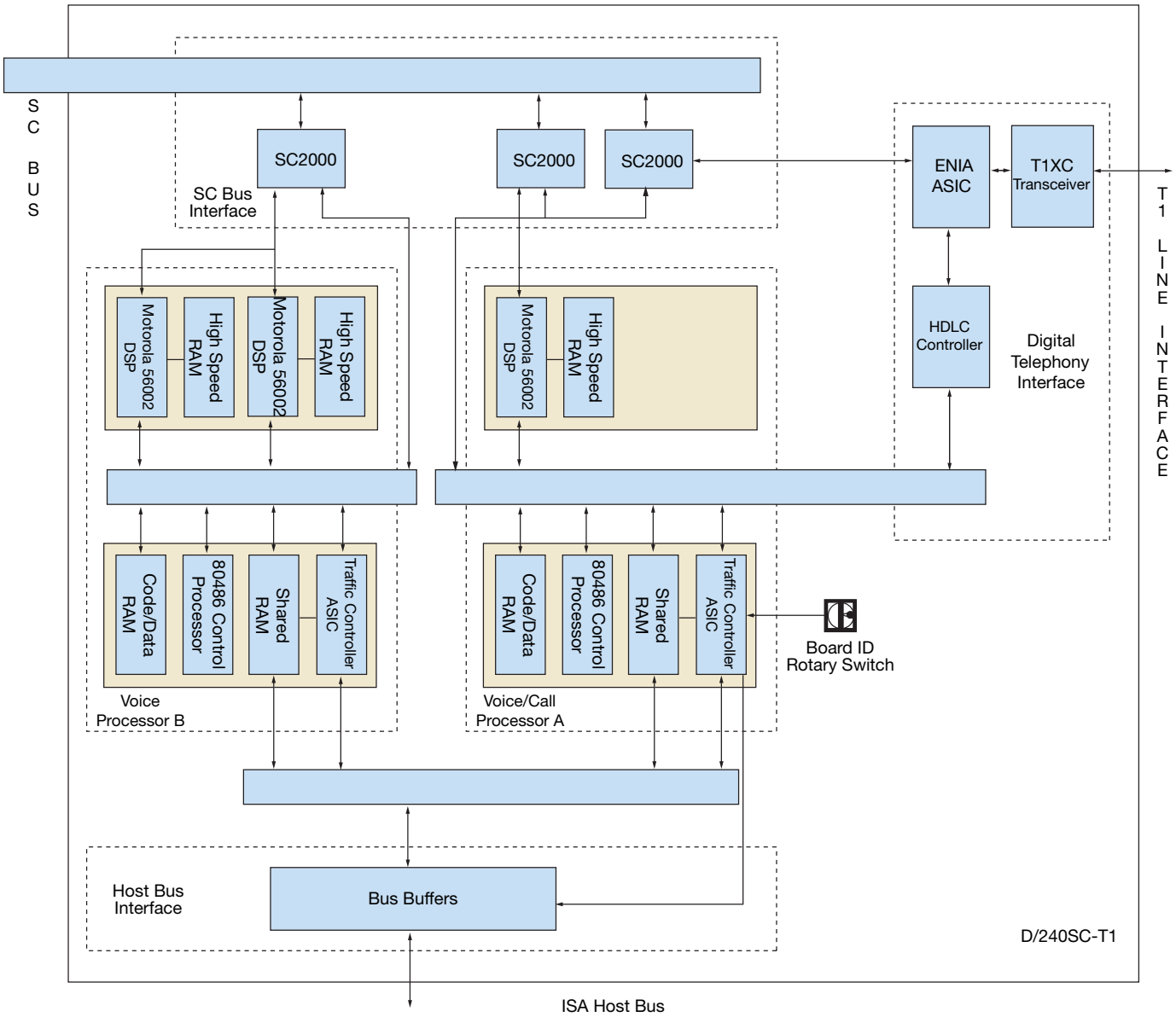
D/240PCI-T1 and D/240SC-T1

Both the Intel Dialogic D/240PCI-T1 and D/240SC-T1 voice boards connect directly to a channel service unit (CSU), digital service unit (DSU), or to other network terminating equipment. The CSU chosen must support the D4 or ESF (within ISDN) superframe format. Most functions traditionally performed by a DSU (such as unipolar to bipolar format conversion, framing, etc.) are performed by the D/240PCI-T1 or D/240SC-T1 board. The only exception is the ability to interpret certain bipolar violation patterns, such as loopback start and stop commands from the T-1 network.

Both boards process the digital on-hook/off-hook signaling information and digital voice signals from the telephone network. Digital T-1 signals enter the board via a T1XC line interface (see block diagrams). The line interface contains a software switchable clock that can be set to

- Loop (clocking is slaved to the external network)
- Independent (clocking is derived from an onboard oscillator)
- Expansion (clocking is slaved to another bus clock master board)

The incoming T-1 bit stream is applied to an SC2000 chip that acts as a traffic coordinator for each channel and as



D/240SC-T1 Block Diagram

an interface to the SCbus. This serial bit stream contains the digitized voice data and the signaling information for the incoming call.

Each of three SC2000 chips on the D/240SC-T1 board (or two SC2002 in the case of the D/240PCI-T1 board) transmit several lower speed data streams over a single high-speed channel. The bus configuration is set when the firmware is downloaded at system initialization. These chips incorporate matrix switching capabilities. Under control of an onboard control processor, an SC2000 chip can connect a call being processed or an available external resource to any of the 1024 SCbus time slots.

(The D/240SC-T1 board can also connect to 24 PCM Expansion Bus [PEB] time slots.) This lets the application route calls to any added resource, such as fax, TTS, or ASR.

A DSP resource receives digital voice data via an SC2000 module. The DSP processes the digitized voice data based on Spring Ware firmware loaded in its high-speed RAM. Each DSP performs the following signal analysis and operations on this incoming data:

- Performs automatic gain control (AGC) to compensate for variations in the level of the incoming audio signal

- Applies an ADPCM or G.711 PCM algorithm to compress the digitized voice and save disk storage space
- Detects the presence of tones — DTMF, MF, or an application-defined single- or dual-frequency tone
- Detects silence to determine whether the line is quiet and the caller is not responding

For outbound data, the DSP performs the following operations:

- Expands stored, compressed audio data for playback
- Adjusts the volume and rate of speed of playback upon application or user request
- Generates tones — DTMF, MF, or any application-defined general-purpose tone

The dual processor combination also performs the following outbound dialing and call progress monitoring functions:

- Transmits an off-hook signal to the telephone network
- Dials out (makes an outbound call)
- Monitors and reports call progress results
  - — line busy or congested
  - — operator intercept
  - — ring, no answer
  - — or if the call is answered, whether answered by a person, an answering machine, a facsimile, or a modem

When recording speech, the DSP can use different digitizing rates from 24 Kb/s to 64 Kb/s as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis and can be changed each time a record or play function is initiated. The DSP processed speech is transmitted by the control processor to the host PC for disk storage. When playing back a stored file, the processor retrieves the voice information from the host PC and passes it to the DSP, which converts the file into digitized voice. The DSP uses the SCbus circuitry to send the digitized voice responses to the caller via the T1XC line interface.

For SCbus configurations, the internal local bus operates at 2.048 Mb/s. For D/240SC-T1 PEB configurations, the external PEB and the internal local bus operate at 1.544 Mb/s.

The High-Level Data Link Controller (HDLC) formats ISDN data. The HDLC receives ISDN signaling data from the T1XC interface and the Enhanced Network Interface ASIC (ENIA) and makes it available to the control processor. It also formats and sends outbound signaling data from the control processor to the network interface through the ENIA ASIC and T1XC transceiver chip.

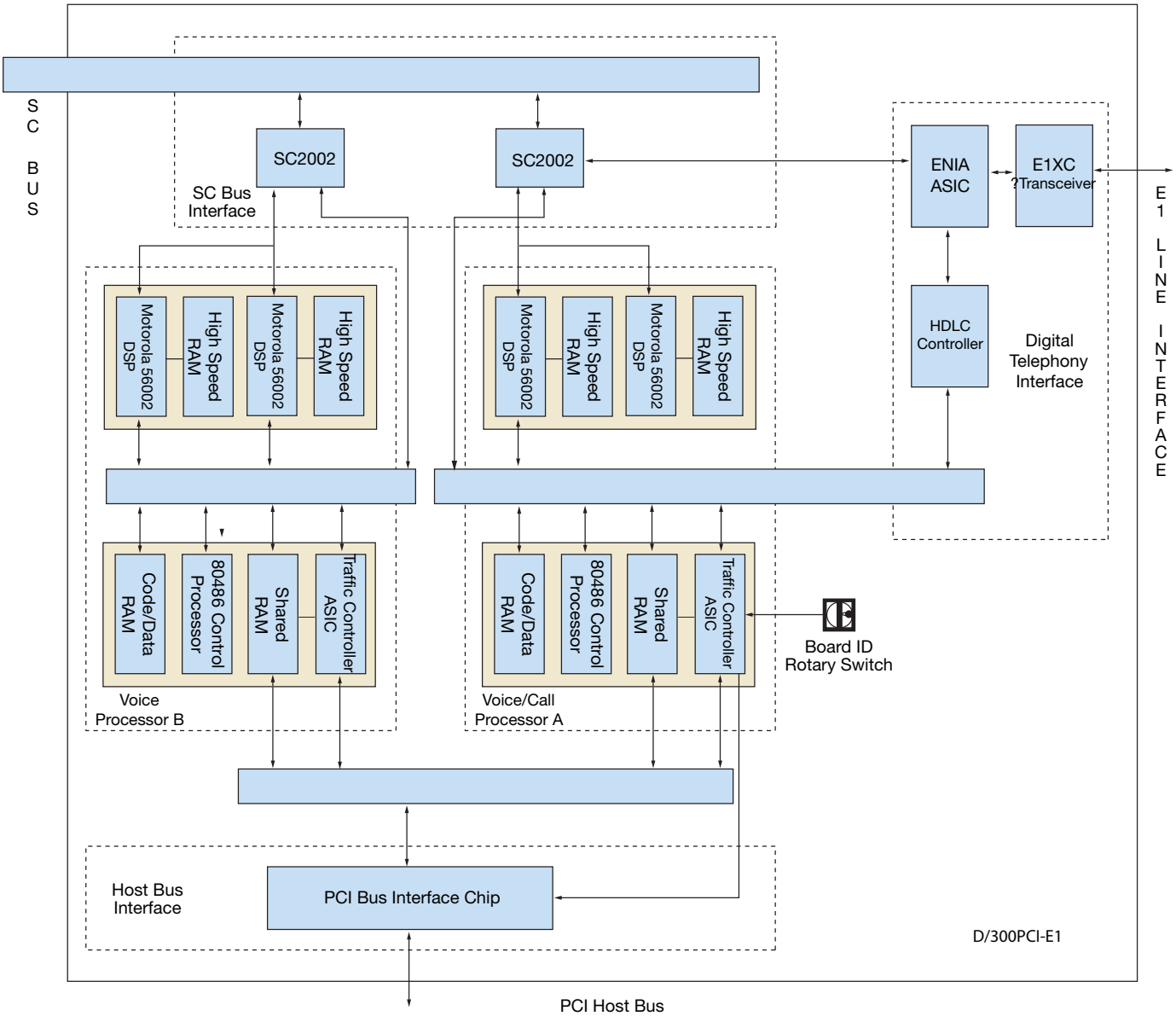
The onboard control processor(s) controls all operations of the board via a local bus and interprets and executes commands from the host PC. These processors handle real-time events, manage data flow to the host PC to provide faster system response time, reduce PC host processing demands, process DTMF and telephony signaling before passing them to the application, and free the DSPs to perform signal processing.

Communications between a processor and the host PC is via the shared RAM that acts as an input/output buffer and thus increases the efficiency of disk file transfers. This RAM interfaces to the host PC via the PCI bus in the case of the D/240PCI-T1 board or the ISA bus in the case of the D/240SC-T1 board. All operations are interrupt-driven to meet the demands of real-time systems. When the system is initialized, Spring Ware firmware is downloaded from the host PC to the onboard code/data RAM and DSP RAM to control all board operations. This downloadable firmware gives the board all of its intelligence and permits easy feature enhancement and upgrades.

The Traffic Controller ASIC is the Intel486 processor interface that handles all peripheral devices (SC2000, HDLC, DSPs, T1XC) and host PC functions (board locator technology, programmable interrupts [ISA only] and shared RAM). The board locator technology circuit inside the Traffic Controller ASIC operates in conjunction with a rotary switch, eliminating the need to set confusing jumpers or DIP switches. The board locator technology is used to map all T-1 boards' shared RAM to the same PC memory space.

D/300PCI-E1 and D/300SC-E1

Both the Intel Dialogic D/300PCI-E1 and D/300SC-E1 boards process the digital on-hook/off-hook signaling information and digital voice signals from the telephone network. Digital E-1 signals enter the board via an E1XC line interface (see block diagrams). The line interface sup-

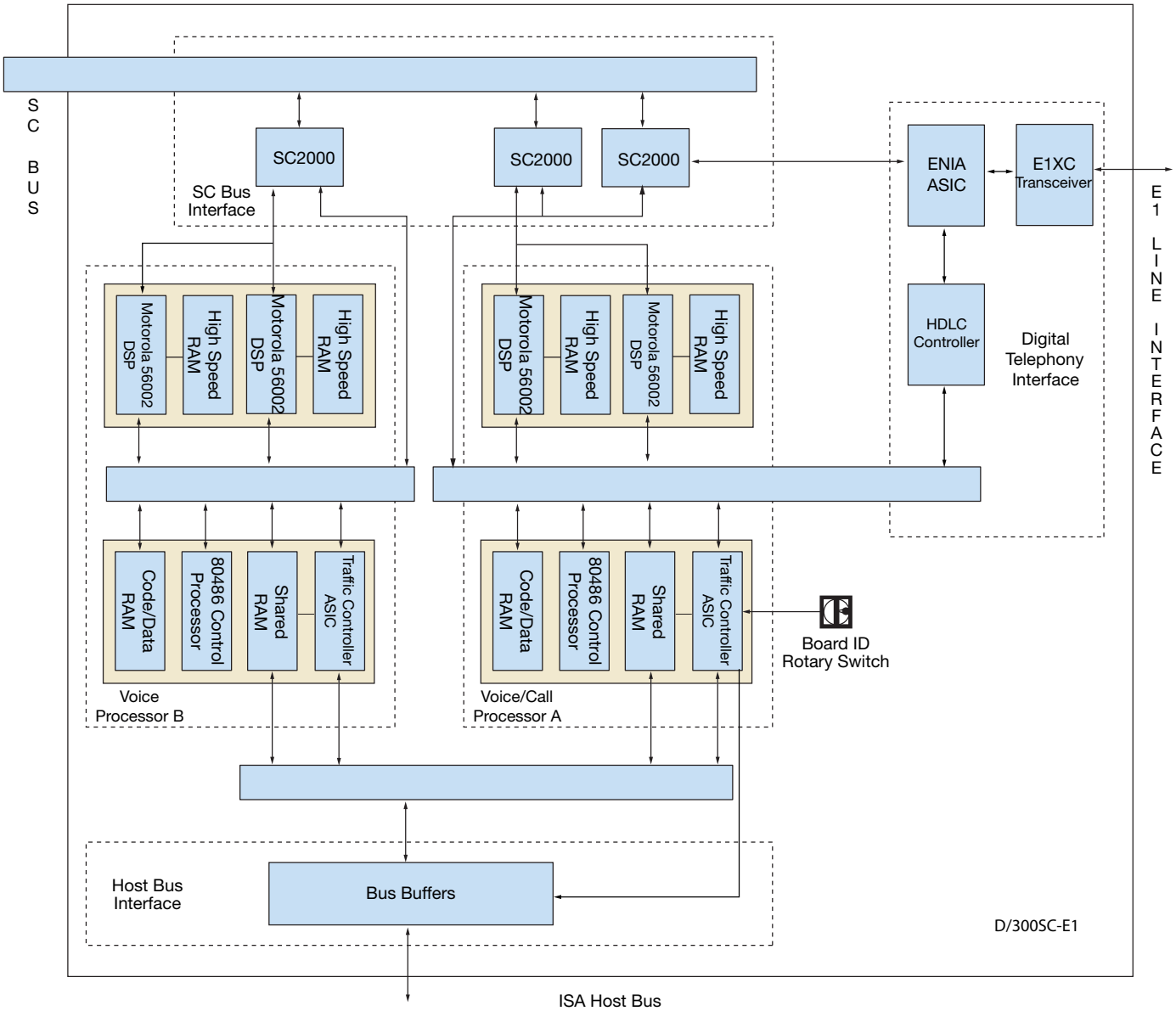


D/300PCI-E1 Block Diagram

ports CRC4 error detection (Cyclic Redundancy Check) and contains a software switchable clock that can be set to

- Loop (clocking is slaved to the external network)
- Independent (clocking is derived from an onboard oscillator)
- Expansion (clocking is slaved to another bus clock master board)

Each of three SC2000 chips on the D/300SC-E1 board (or two SC2002 in the case of the D/300PCI-E1 board) transmit several lower speed data streams over a single high-speed channel. The bus configuration is set when the firmware is downloaded at system initialization. These chips incorporate matrix switching capabilities. Under control of an onboard control processor, an SC2000 chip can connect a call being processed or an available external resource to any of the 1024 SCbus time slots. This lets the application route calls to any added resource, such as fax, TTS, or ASR.



D/300SC-E1 Block Diagram

A DSP resource receives digital voice data via an SC2000 module. The DSP processes the digitized voice data based on Spring Ware firmware loaded in its high-speed RAM. Each DSP performs the following signal analysis and operations on this incoming data:

- Performs AGC to compensate for variations in the level of the incoming audio signal
- Applies an ADPCM or G.711 PCM algorithm to compress the digitized voice and save disk storage space
- Detects the presence of tones — DTMF, R2MF, or application-defined single- or dual- frequency tone
- Detects silence to determine whether the line is quiet and the caller is not responding

For outbound data, the DSP performs the following operations:

- Expands stored, compressed audio data for playback
- Adjusts the volume and rate of speed of playback upon application or user request
- Generates tones — DTMF, R2MF, or any application-defined general-purpose tone

The dual processor combination also performs the following outbound dialing and call progress monitoring functions:

- Transmits an off-hook signal to the telephone network
- Dials out (makes an outbound call)
- Monitors and reports call progress results
  - line busy or congested
  - operator intercept
  - ring, no answer
  - or if the call is answered, whether answered by a person, an answering machine, a facsimile, or a modem

The board's line interface extracts or inserts telephony signaling information, which an onboard control processor processes. The DSPs only process the digitized voice data.

When recording speech, the DSP can use different digitizing rates from 24 Kb/s to 64 Kb/s as selected by the application for the best speech quality and most efficient storage. The digitizing rate is selected on a channel-by-channel basis and can be changed each time a record or play function is initiated. The DSP processed speech is transmitted by the control processor to the host PC for disk storage. When playing back a stored file, the processor retrieves the voice information from the host PC and passes it to the DSP, which converts the file into digitized voice. The DSP sends the digitized voice responses to the caller via the SC2000 functional modules, the SCbus, and the E1XC line interface.

The HDLC formats ISDN data. The HDLC receives ISDN signaling data from the E1XC interface and the ENIA and makes it available to the control processor. It also formats and sends outbound signaling data from the control processor to the network interface through the ENIA ASIC and E1XC transceiver chip.

The onboard control processor(s) controls all operations of the board via a local bus and interprets and executes commands from the host PC. These processors handle real-time events, manage data flow to the host PC to provide faster system response time, reduce PC host processing demands, process DTMF and telephony signaling before passing them to the application, and free the DSPs to perform signal processing.

Communications between a processor and the host PC is via the shared RAM that acts as an input/output buffer and thus increases the efficiency of disk file transfers. This RAM interfaces to the host PC via the PCI bus in the case of the D/300PCI-E1 board or the ISA bus in the case of the D/300SC-E1 board. All operations are interrupt-driven to meet the demands of real-time systems. When the system is initialized, Spring Ware firmware is downloaded from the host PC to the onboard code/data RAM and DSP RAM to control all board operations. This downloadable firmware gives the board all of its intelligence and permits easy feature enhancement and upgrades.

The Traffic Controller ASIC is the Intel486 processor interface that handles all peripheral devices (SC2000, HDLC, DSPs, E1XC) and host PC functions (board locator technology, programmable interrupts [ISA only], and shared RAM). The board locator technology circuit inside the Traffic Controller ASIC operates in conjunction with a rotary switch, eliminating the need to set confusing jumpers or DIP switches. The board locator technology is used to map all E-1 boards' shared RAM to the same PC memory space.

Technical Specifications

D/240PCI-T1

Number of ports	24
Max. boards/system	16. Number may be limited by application and system performance
Digital network interface	Onboard DSX-1 interface
Resource sharing bus	CT Bus operating in SCbus mode
Control microprocessor	Two Intel486™ GX processors @ 28.5 MHz, 0 wait state
Digital signal processors	Three Motorola* DSP56002 @ 49 MHz to 66 MHz, each with 64 K word private, 0 wait state SRAM

Host Interface

Bus compatibility	PCI. Complies with PCISIG Bus Specification, Rev. 2.2
Bus speed	33 MHz max.
Bus mode	32- to 16-bit conversion in target mode
Shared memory	64 KB page
I/O ports	None

Telephone Interface

Clock rate	1.544 Mb/s ±32 ppm
Level	3.0 V (nominal)
Pulse width	323.85 ns (nominal)
Line impedance	100 Ohm ±10%
Other electrical characteristics	Complies with AT&T* TR62411 and ANSI T1.403-1989
Framing	SF (D3/D4) ESF for ISDN
Line coding	AMI AMI with B7 stuffing B8ZS
Clock and data recovery	Complies with AT&T TR62411 and Bellcore* TA-TSY-000170
Jitter tolerance	Complies with AT&T TR62411 and ANSI T1.403-1989
Connectors	RJ-48C
Telephony bus connector	H.100-style 68-pin fine pitch card edge connector
Loopback	Supports switch-selectable local analog loopback and software-selectable local digital loopback

Power Requirements

+5 VDC	2.3 A typical; 2.8 A max.
+12 VDC	30 mA typical; 40 mA max.
–12 VDC	30 mA typical; 40 mA max.
Operating temperature	0°C to +50°C
Storage temperature	–20°C to +70°C
Humidity	8% to 80% noncondensing
Form factor	PC AT 12.3 in. (30.75 cm) long (without edge retainer) or 13.3 in. (33.25 cm) long (with edge retainer) 0.79 in. (1.98 cm) wide (total envelope) 3.87 in. (9.675 cm) high (excluding edge connector)

Safety and EMI Certifications

Approvals	For country-specific approval information, see the Global Product Approvals list at http://resource.intel.com/globalapproval/globalapproval.asp
Estimated MTBF	150,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Technical Specifications (cont.)

D/240SC-T1

Number of ports	24
Max. boards/system	16. Number may be limited by application and system performance
Digital network interface	Onboard DSX-1 interface
Resource sharing bus	SCbus with PEB connectors
Control microprocessor	Two Intel486 GX processors @ 28.5 MHz, 0 wait state
Digital signal processors	Three Motorola DSP56002 @ 49 MHz to 66 MHz, each with 32 K word private, 0 wait state SRAM

Host Interface

Bus compatibility	IEEE P996 ISA compatible (IBM PC AT)
Bus speed	8 MHz typical
Bus mode	Automatically configures to 8- or 16-bit transfer mode
Shared memory	32 KB page
Base addresses	8000h to E800h, on 32 K boundaries. All boards share the same base address. Shared memory is page mapped in/out dynamically as needed.
Interrupt level	IRQ 2/9, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15, software selectable. One IRQ line must be shared by all boards.
I/O ports	None

Telephone Interface

Clock rate	1.544 Mb/s ±32 ppm
Level	3.0 V (nominal)
Pulse width	323.85 ns (nominal)
Line impedance	100 Ohm ±10%
Other electrical characteristics	Complies with AT&T TR62411 and ANSI T1.403-1989
Framing	SF (D3/D4) ESF for ISDN
Line coding	AMI AMI with B7 stuffing B8ZS
Clock and data recovery	Complies with AT&T TR62411 and Bellcore TA-TSY-000170
Jitter tolerance	Complies with AT&T TR62411 and ANSI T1.403-1989
Connectors	RJ-48C
Loopback	Supports switch-selectable local analog loopback and software-selectable local digital loopback

Power Requirements

+5 VDC	2.1 A typical; 2.5 A max.
+12 VDC	30 mA typical; 40 mA max.
–12 VDC	30 mA typical; 40 mA max.
Operating temperature	0°C to +50°C
Storage temperature	–20°C to +70°C
Humidity	8% to 80% noncondensing
Form factor	PC AT 13.3 in. (33.25 cm) long 0.793 in. (1.98 cm) wide (total envelope) 4.5 in. (11.25 cm) high (excluding edge connector)

Safety and EMI Certifications

Approvals	For country-specific approval information, see the Global Product Approvals list at http://resource.intel.com/globalapproval/globalapproval.asp
Estimated MTBF	269,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Technical Specifications (cont.)

D/300PCI-E1

Number of ports	30
Max. boards/system	16. Number may be limited by application and system performance
Digital network interface	Onboard E-1 interface
Resource sharing bus	CT Bus operating in SCbus mode
Control microprocessor	Two Intel486 GX processors @ 28.5 MHz, 0 wait state
Digital signal processors	Four Motorola DSP56002 @ 49 MHz to 66 MHz, each with 64 K word private, 0 wait state SRAM

Host Interface

Bus compatibility	PCI. Complies with PCISIG Bus Specification, Rev 2.2.
Bus speed	33 MHz max.
Bus mode	32- to 16-bit conversion in target mode
Shared memory	64 KB page
I/O ports	None

Telephone Interface

Network clock rate	2.048 Mb/s ±50 ppm
Internal clock rate	2.048 Mb/s ±32 ppm
Level	2.37 V (nominal) for 75 Ohm lines 3.0 V (nominal) for 120 Ohm lines
Pulse width	244 ns (nominal)
Line impedance	75 Ohm, unbalanced 120 Ohm, balanced
Other electrical characteristics	Complies with CCITT Rec G.703
Framing	CCITT G.704-1988 with CRC4
Line coding	HDB3
Clock and data recovery	Complies with CCITT Rec. G.823-1988
Jitter tolerance	Complies with CCITT Rec. G.823, G.737, G.739, G.742-1988
Connectors	BNC for 75 Ohm lines RJ-48C for 120 Ohm lines
Telephony bus connector	H.100-style 68-pin fine pitch card edge connector
Loopback	Supports switch-selectable local analog loopback and software-selectable local digital loopback

Power Requirements

+5 VDC	2.3 A typical; 2.8 A max.
+12 VDC	30 mA typical; 40 mA max.
–12 VDC	30 mA typical; 40 mA max.
Operating temperature	0°C to +50°C
Storage temperature	–20°C to +70°C
Humidity	8% to 80% noncondensing
Form factor	PC AT 12.3 in. (30.75 cm) long (without edge retainer) or 13.3 in. (33.25 cm) long (with edge retainer) 0.79 in. (1.98 cm) wide (total envelope) 3.87 in. (9.675 cm) high (excluding edge connector)

Safety and EMI Certifications

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Estimated MTBF	150,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Technical Specifications (cont.)

D/300SC-E1

Number of ports	30
Max. boards/system	16. Number may be limited by application and system performance
Digital network interface	Onboard E-1 interface
Resource sharing bus	SCbus with PEB connectors
Control microprocessor	Two Intel486 GX processors @ 32.768 MHz, 0 wait state
Digital signal processors	Four Motorola DSP56002 @ 49 MHz to 66 MHz, each with 32 K word private, 0 wait state SRAM

Host Interface

Bus compatibility	IEEE P996 ISA compatible (IBM PC AT)
Bus speed	8 MHz typical
Bus mode	Automatically configures to 8- or 16-bit transfer mode
Shared memory	32 KB page
Base addresses	8000h to E800h, on 32 K boundaries. All boards share the same base address. Shared memory is page mapped in/out dynamically as needed.
Interrupt level	IRQ 2/9, 3, 4, 5, 6, 7, 10, 11, 12, 14, 15, software selectable. One IRQ line must be shared by all boards.
I/O ports	None

Telephone Interface

Network clock rate	2.048 Mb/s ±50 ppm
Internal clock rate	2.048 Mb/s ±32 ppm
Level	2.37 V (nominal) for 75 Ohm lines 3.0 V (nominal) for 120 Ohm lines
Pulse width	244 ns (nominal)
Line impedance	75 Ohm, unbalanced 120 Ohm, balanced
Other electrical characteristics	Complies with CCITT Rec G.703
Framing	CCITT G.704-1988 with CRC4
Line coding	HDB3
Clock and data recovery	Complies with CCITT Rec. G.823-1988
Jitter tolerance	Complies with CCITT Rec. G.823, G.737, G.739, G.742-1988
Connectors	BNC for 75 Ohm lines RJ-48C for 120 Ohm lines
Loopback	Supports switch-selectable local analog loopback and software-selectable local digital loopback

Power Requirements

+5 VDC	2.1 A typical; 2.5 A max.
+12 VDC	30 mA typical; 40 mA max.
–12 VDC	30 mA typical; 40 mA max.
Operating temperature	0°C to +50°C
Storage temperature	–20°C to +70°C
Humidity	8% to 80% noncondensing
Form factor	PC AT 13.3 in. (33.25 cm) long 0.793 in. (1.98 cm) wide (total envelope) 4.5 in. (11.25 cm) high (excluding edge connector)

Safety and EMI Certifications

Approvals	For country-specific approval information, see the Global Product Approvals list at http://resource.intel.com/globalapproval/globalapproval.asp
Estimated MTBF	254,000 hours per Bellcore Method I
Warranty	Intel® Telecom Products Warranty Information at http://www.intel.com/network/csp/products/3144web.htm

Spring Ware Firmware Technical Specifications

Audio Signal		
	Receive range	(T-1) –40 dBm0 to +2.5 dBm0 nominal, configurable by parameter† (E-1) –43 dBm0 to +2.5 dBm0 nominal, configurable by parameter†
	Automatic gain control	Application can enable/disable. Above –18 dBm0 (T-1) or –21 dBm0 (E-1) results in full-scale recording, configurable by parameter.†
	Silence detection	–38 dBm0 nominal, software adjustable†
	Transmit level (weighted average)	(T-1) –9 dBm0 nominal, configurable by parameter† (E-1) –12.5 dBm0 nominal, configurable by parameter†
	Transmit volume control	40 dB adjustment range, with application-definable increments and legal limit cap
Frequency Response		
	24 Kb/s	300 Hz to 2600 Hz ±3 dB
	32 Kb/s	300 Hz to 3400 Hz ±3 dB
	48 Kb/s	300 Hz to 2600 Hz ±3 dB
	64 Kb/s	300 Hz to 3400 Hz ±3 dB
Audio Digitizing		
	24 Kb/s	OKI ADPCM @ 6 kHz sampling
	32 Kb/s	OKI ADPCM @ 8 kHz sampling
	48 Kb/s	A-law G.711 PCM @ 6 kHz sampling
	64 Kb/s	A-law G.711 PCM @ 8 kHz sampling
	48 Kb/s	μ-law G.711 PCM @ 6 kHz sampling
	64 Kb/s	μ-law G.711 PCM @ 8 kHz sampling
	Digitization selection	Selectable by application on function call-by-call basis
	Playback speed control	Pitch controlled Available for 24 and 32 Kb/s data rates Adjustment range: ±50% Adjustable through application or programmable DTMF control
DTMF Tone Detection		
	DTMF digits	0 to 9, *, #, A, B, C, D per CCITT Q.23
	Dynamic range	–36 dBm0 to –3 dBm0 (T-1) or –39 dBm0 to 0 dBm0 (E-1) per tone, configurable by parameter†
	Minimum tone duration	40 ms, can be increased with software configuration
	Interdigit timing	Detects like digits with a >40 ms interdigit delay Detects different digits with a 0 ms interdigit delay
	Acceptable twist and frequency variation	(T-1) Meets Bellcore LSSGR Sec 6 and EIA 464 requirements (E-1) Meets appropriate CCITT specifications†
	Noise tolerance	Meets Bellcore LSSGR Sec 6 and EIA 464 requirements for Gaussian, impulse, and power line noise tolerance
	Cut-through	(T-1) Local echo cancellation permits 100% detection with a >4.5 dB return loss line. (E-1) Digital trunks use separate transmit and receive paths to network. Performance dependent on far-end handset's match to local analog loop.
	Talk off	Detects less than 20 digits while monitoring Bellcore TR-TSY-000763 standard speech tapes. (LSSGR requirements specify detecting no more than 470 total digits.) Detects 0 digits while monitoring MITEL speech tape #CM 7291.

Spring Ware Firmware Technical Specifications (cont.)

Global Tone Detection		
	Tone type	Programmable for single or dual
	Max. number of tones	Application-dependent
	Frequency range	Programmable within 300 Hz to 3500 Hz
	Max. frequency deviation	Programmable in 5 Hz increments
	Frequency resolution	±5 Hz. Separation of dual frequency tones is limited to 62.5 Hz at a signal-to-noise ratio of 20 dB.
	Timing	Programmable cadence qualifier, in 10 ms increments
	Dynamic range	(T-1) Programmable, default set at –36 dBm0 to –0 dBm0 (single tone), –3 dBm0 (dual tone) (E-1) Programmable, default set at –39 dBm0 to +0 dBm0 per tone
Global Tone Generation		
	Tone type	Generate single or dual tones
	Frequency range	Programmable within 200 Hz to 4000 Hz
	Frequency resolution	1 Hz
	Duration	10 ms increments
	Amplitude	(T-1) –43 dBm0 to –3 dBm0 per tone nominal, programmable (E-1) –40 dBm0 to +0 dBm0 per tone nominal, programmable
MF Signaling (T-1)	**R1**	
	MF digits	0 to 9, KP, ST, ST1, ST2, ST3 per Bellcore LSSGR Sec 6, TR-NWT-000506 and CCITT Q.321
	Transmit level	Complies with Bellcore LSSGR Sec 6, TR-NWT-000506
	Signaling mechanism	Complies with Bellcore LSSGR Sec 6, TR-NWT-000506
	Dynamic range for detection	–25 dBm0 to –3 dBm0 per tone
	Acceptable twist	6 dB
	Acceptable freq. variation	Less than ±1 Hz
MF Signaling (E-1)	**R2**	
	MF digits	All 15 forward and backward signal tones per CCITT Q.441
	Transmit level	–8 dBm0 per tone, nominal, per CCITT Q.454; programmable
	Signaling mechanism	Supports the R2 compelled signaling cycle and non-compelled pulse requirements per CCITT Q.457 and Q.442
	Dynamic range for detection	–35 dBm0 to –5 dBm0 per tone
	Acceptable twist	6 dB
	Acceptable freq. variation	Less than ±1 Hz
Call Progress Analysis		
	Busy tone detection	Default setting designed to detect 74 out of 76 unique busy/congestion tones used in 97 countries as specified by CCITT Rec. E., Suppl. #2. Default uses both frequency and cadence detection. Application can select frequency only for faster detection in specific environments.
	Ring back detection	Default setting designed to detect 83 out of 87 unique ring back tones used in 96 countries as specified by CCITT Rec. E., Suppl. #2. Uses both frequency and cadence detection.
	Positive voice detection accuracy	99% based on tests on a database of real world calls in North America. Performance in other markets may vary.
	Positive voice detection speed	Detects voice in as little as 1/10th of a second
	Positive answering machine detection accuracy	85% based on tests on a database of real world calls in North America. Performance in other markets may vary.
	Fax/modem detection	Preprogrammed
	Intercept detection	Detects entire sequence of the North American tri-tone. Other intercept tone sequences can be programmed.
	Dial tone detection before dialing	Application enable/disable Supports up to three different user-definable dial tones Programmable dial tone drop out debouncing

Spring Ware Firmware Technical Specifications (cont.)

Tone Dialing		
	DTMF digits	0 to 9, *, #, A, B, C, D per Bellcore LSSGR Sec 6, TR-NWT-000506
	Frequency variation	Less than ±1 Hz
	Rate	10 digits/s, configurable by parameter†
	Level	–7.5 dBm0 per tone, nominal, configurable by parameter†
Pulse Dialing		
	10 digits	0 to 9
	Pulsing rate	10 pulses/s, nominal, configurable by parameter†
	Break ratio	60% nominal, configurable by parameter†
Analog Display Services Interface (ADSI)		
		FSK generation per Bellcore TR-NWT-000030
		CAS tone generation and DTMF detection per Bellcore TR-NWT-001273

Hardware System Requirements

D/240PCI-T1 and D/300PCI-E1

- Intel386, Intel486, or Pentium processor PCI bus or mixed PCI/ISA bus computer
- Operating system hardware requirements vary according to the number of channels being used
- System must comply with PCISIG Bus Specification Rev. 2.2 or later

D/240SC-T1 and D/300SC-E1

- Intel386, Intel486, or Pentium processor IBM PC AT (ISA) bus or compatible computer
- Operating system hardware requirements vary according to the number of channels being used

Additional Components (with Item Market Name)

D/240PCI-T1 and D/300PCI-E1

- Multidrop CT Bus cables (CBLCTB68C3DROP, CBLCTB68C4DROP, CBLCTB68C8DROP, CBLCTB68C12DROP, CBLCTB68C16DROP)
- CT Bus/SCbus adapter (CTBUSTOSCBUSADP)
- SCbus terminator kits (1SCBUS1TERMKIT, 2SCBUS1TERMKIT, 3SCBUS1TERMKIT)

D/240SC-T1 and D/300SC-E1

- Multidrop SCbus cables (CBLPEBSCB4DROP, CBLPEBSCB8DROP, CBLPEBSCB12DROP, CBLPEBSCB16DROP)
- Multidrop PEB cables (CBLPEB26C2DROP, CBLPEB26C3DROP, CBLPEB26C4DROP, CBLPEB26C5DROP, CBLPEB26C6DROP, CBLPEB26C8DROP, CBLPEB26C10DROP)
- CT Bus/SCbus adapter (CTBUSTOSCBUSADP)
- SCbus terminator kits (1SCBUS1TERMKIT, 2SCBUS1TERMKIT, 3SCBUS1TERMKIT)

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Positive Answering Machine Detection/Positive Voice Detection
These performance results were measured using specific computer systems and/or components within specific lab environments and under specific system configurations. Any difference in system hardware, software design, or configuration may affect actual performance. The results are furnished for informational use only and should not be construed as a commitment by Intel. Intel assumes no responsibility or liability for any errors or inaccuracies.

Outbound Dialing/Telemarketing
Outbound dialing systems may be subject to certain laws or regulations. Intel makes no representation that Intel products will satisfy the requirements of any such laws or regulations (including, without limitation, any regulations dealing with telemarketing).

†Configurable to meet country specific PTT requirements. Actual specification may vary from country to country for approved products.

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